IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

	ATTY. DOCKET NO.:	**RPS920030151US1**
IN RE APPLICATION OF:	§	
	§	
KENNETH DOCKSER	§ EXAMINER:	**BRIAN P. JOHNSON**
	§	
SERIAL NO.: **10/699,571**	§ CONFIRMATION NO.:	**1590**
	§	
FILED: **OCTOBER 31, 2003**	§ ART UNIT:	**2183**
	§	
FOR: **VECTOR EXECUTION UNIT TO PROCESS A VECTOR INSTRUCTION BY EXECUTING A FIRST OPERATION ON A FIRST SET OF OPERANDS AND A SECOND OPERATION ON A SECOND SET OF OPERANDS**	§	

APPEAL BRIEF UNDER 37 C.F.R. 41.37

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Alexandria, Virginia 22313-1450

Sir:

This Compliant Appeal Brief is submitted in response to a Notification of Non-Compliant Appeal mailed on May 17, 2007, for the Appeal Brief filed on May 2, 2007.

No fee is required to submit this Compliant Appeal Brief as the fee for filing the original Appeal Brief was paid at submission. However, should any fees be required to file this Compliant Appeal Brief, please charge that fee, as well as any additional required fees, to **IBM CORPORATION's Deposit Account No. 50-0563.**

REAL PARTY IN INTEREST

The real party in interest in the present Application is International Business Machines Corporation, the Assignee of the present application as evidenced by the Assignment set forth at reel 014474, frame 0057.

RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellants, the Appellants' legal representative, or assignee, which directly affect or would be directly affected by or have a bearing on the Board's decision in the pending appeal.

STATUS OF CLAIMS

Claims 1, 4, 7-9, 21-34 stand finally rejected by the Examiner as noted in the Final Office Action dated February 9, 2007. The rejection of Claims 1, 4, 7-9, 21-34 is appealed.

STATUS OF AMENDMENTS

Appellants' Amendment B, filed on January 19, 2007 was entered by the Examiner, as noted in the Final Office Action. No amendments were filed subsequent to the Final Office Action from which this Appeal is taken.

SUMMARY OF THE CLAIMED SUBJECT MATTER

Applicants' invention provides a mechanism and (asymmetric) instruction that enables vector-type processing (in parallel) on two sets of three operands, where the processing/operations on each set of three operands are different. The vector register file 201, has a rank of two (page 4, line 7-9). Each set of three operands are retrieved from a pair of primary and secondary registers, via multiplexers, which enable reordering or replicating of data from both registers, where the data is selected based on a select signal from the opcode. The vector unit 200 enables "cross-type arithmetic instructions and asymmetric instructions using a single instruction" (page 6, line 20-21). The vector unit 200 includes a pair of 3-input arithmetic units, a primary ALU 220 and a secondary ALU 230 that receives an A, B and C input from respective A, B and C multiplexers (page 6, lines 21-31). The "arrangement of multiplexers

beneficially enables primary side ALU 220 and secondary ALU 230 to select inputs from either side of vector register file 201 (page 7, lines 1-2).

As recited by example Claim 1, Appellant's invention provides: [a] microprocessor **100** (FIG. 1; pages 4-5), comprising: a vector unit **200** (FIGs. 1 and 2) to execute a vector instruction **300** (FIG. 3) to perform a first operation on a first set of operands and a second operation on a second set of operands (page 3, lines 30 – page 4, line 2); a vector register file **201** comprising a primary register file **202** and a secondary register file **204** (page 4, lines 7 – 10); wherein the vector instruction **300** includes a first register field (**306**) indicative of a first primary register in the primary register file **202** and a first secondary register in the secondary register file **204**, a second register field (**308**) indicative of a second primary register in the primary register file **202** and a second secondary register in the secondary register file **204**, and a third register field (**310**) indicative of a third primary register in the primary register file **202** and a third secondary register in the secondary register file **204** (see page 6, lines 1 - 5); and wherein the first set of operands includes a first operand selected from the first primary register or the first secondary register, a second operand selected from the second primary register or the second secondary register, and a third operand selected from the third primary register or the third secondary register (*see* pages 4 – 5; page 6, line 19 – page 7, line 3).

Example Claim 4 further provides: wherein the vector unit **200** includes a 3-input primary unit **220** and a 3-input secondary unit **230**, wherein the primary unit **220** is configured to perform the first operation on the first set of operands and the 3-input secondary unit **230** is configured to perform the second operation on the second set of operands (*see* page 6, lines 19 – page 7, line 3).

Example Claim 25 provides: [a] vector unit **205** to process a vector instruction **300** having an opcode **302-1**, **302-2** and first, second, and third register fields (**306**, **308**, **310**) comprising: a register file including a primary register file **202** having a set of primary registers and a secondary register file **204** having a set of secondary registers (page 4, lines 7 – 10), wherein each register field identifies a register in the primary register file **202** and a corresponding register in the secondary register file **204**; primary and secondary calculating

units **220/230**, wherein the primary calculating unit **220** includes first, second, and third inputs to receive, respectively, first, second, and third operands of a first set of operands and wherein the secondary calculating unit **230** includes first, second, and third inputs to receive, respectively, first, second, and third operands of a second set of operands (page 6, line 19 – page 7, line 3; and multiplexing circuitry **(222-236)** controlled by the opcode to select each of the first, second, and third operands in the first and second set of operands from the set of primary and secondary file registers identified by the register fields (*id.*).

Finally, example Claim 31 provides: [a] microprocessor **(100)** including: an execution unit **200** enabled to execute an asymmetric instruction **300**, wherein the asymmetric instruction **300** includes a set of three operand register fields **(306, 308, 310)** and a target register field and an operation code (opcode) **302-1, 302-2**; a register file **201** accessible by the execution unit **200** and having a rank of two including a primary register file **202** and a secondary register file **203** wherein a value in an operand register field identifies a register in the primary register file **202** and a corresponding register in the secondary register file **204**; wherein the execution unit **200** is configured to perform a first operation on a first set of three operands selected from registers identified by the set of operand register fields and to perform a second operation on a second set of three operands also selected from the registers identified by the set of operand registers fields wherein the first and second operations and selection of the first and second sets of operands are determined by the opcode **302-1, 302-2** (*see* page 6, lines 19 – page 7, line 3).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. The Examiner's rejection of Claims 1, 7-9, 21, 23 and 24 under 35 U.S.C. §102(b) as being anticipated by *Wang et al.* (U.S. Patent No. 5,187,769) is to be reviewed on Appeal.

B. The Examiner's rejection of Claims 4, 22 and 25-34 under 35 U.S.C. 103(a) as being unpatentable over *Wang* in view of *Matsuo et al.* (U.S. Patent No. 5,901,301) and the rejection of Claim 10 under 35 U.S.C. 103(a) as being unpatentable over *Wang* in view of *Golliver et al.* (U.S. Pub. No. US 2002/0004809) are to be reviewed on Appeal.

ARGUMENT

A. The rejection of Claims 1, 7-9, 21, 23 and 24 under 35 U.S.C. §102(b) as being anticipated by *Wang et al.* (U.S. Patent No. 5,187,769) is not well founded and should be reversed.

Claims 1 (and 7-9, 21, 23, and 24)

Appellant's exemplary Claim 1 recites, in relevant part:

> (1) the vector instruction includes a **first** register field indicative of a first primary register in the primary register file and a first secondary register in the secondary register file, a **second** register field indicative of a second ..., **and a third** register field indicative of a third ... in the secondary register file (Claim 1, *emphases added*); and
> (2) "the first set of operands includes a first operand selected from the first primary register or the first secondary register, a second operand ..., **and a third operand** selected from the third primary register or the third secondary register" (Claim 1, *emphases added*).

Appellant's claimed invention further provides a vector register file that has a primary register file and a secondary register file, where each register field in the vector instruction indicates a register in the primary register file and a corresponding register in the secondary register file. Thus, a first register field of the instruction identifies a first primary register in the primary register file and a first secondary register in the secondary register file.

The vector unit performs the first operation on a first set of three operands and the second operation on a second set of three operands. Thus, the instruction corresponds to a set of six register operands. The first set of operands includes a first operand chosen from either the first primary or first secondary register, a second operand chosen from either the second primary or second secondary register, and a third operand chosen from the third primary or third secondary registers. In the same way, the second set of operands includes a first operand chosen from either the first primary or first secondary register, a second operand chosen from either the second primary or second secondary register, and a third operand chosen from the third primary or third secondary registers. Thus, all six of the operands are provided from either the primary or secondary register file.

Wang does not anticipate Appellant's Claim 1 because Wang does not describe a vector execution unit for instructions having three operand registers in which all of the operands are provided by a rank-of-two register file (i.e., a register file have a primary register file and a secondary register file), where the selection of the operands occurs from one of six (2x3 registers per file) total register fields within the two register files. Rather, *Wang* provides a vector unit having three separate register files (reference numerals 40, 42, and 44), which each receive a single input.

Also, *Wang*'s illustrated table at col. 27, lines 22-24 provides an instruction naming scheme that enables three-dimensional vector processing. However, that table does not teach the vector instruction having the characteristics and associated functionality of the three register fields within the instruction being respectively indicative of a first/second/third register in the first register file or a first/second/third register in the second register file.

The characteristics and/or functionality associated with the three register fields of the vector instruction is not taught (nor suggested) by *Wang*. Appellant therefore submits that Claim 1 and, by their dependency on Claim 1, Claims 7-9, and 21, 23 and 24, are not anticipated by *Wang*. Accordingly, Appellant respectfully submits that the anticipation rejection of the above Claims is not well founded and should be reversed.

B. The rejections of (1) Claims 4, 22 and 25-34 under 35 U.S.C. 103(a) as being unpatentable over *Wang* in view of *Matsuo et al.* (U.S. Patent No. 5,901,301) and (2) Claim 10 under 35 U.S.C. 103(a) as being unpatentable over *Wang* in view of *Golliver et al.* (U.S. Pub. No. US 2002/0004809) are not well founded and should be reversed.

Claim 4 (10 and 22)

Claim 4 (and 10 and 22) depends from independent Claim 1, which Appellant has shown to be allowable over the primary reference *Wang*. Claim 4 (and 10 and 22), by its dependency on allowable Claim 1, is therefore also allowable over the combination(s) of the primary reference with secondary references, given that the secondary reference(s) also fail to suggest the above features of the independent Claim 1 that *Wang* does not suggest.

Specifically, with respect to example Claim 4, the combination of *Wang* and *Matsuo* does not render Claim 4 unpatentable because one skilled in the art would not find the elements recited by Claim 4 to be obvious at the time of Appellant's invention in light of the combination. Appellant's Claim 4 recites: "the vector unit includes a **3-input primary unit** and a **3-input secondary unit**, wherein the primary unit is configured to perform the first operation on the first set of operands and the 3-input secondary unit is configured to perform the second operation on the second set of operands" (*emphases added*).

Wang is devoid of any teaching (or suggestion) of a pair of 3-input (execution) units. Specifically, *Wang* is devoid of any teaching of (a) **two** sets of **three operands** that feed into (b) **two** respective **3-input units** (3-input primary and 3-input secondary units). Further, *Wang*'s described system does not have a three input execution unit configuration in which the three inputs are retrieved from first, second or third register fields within two register files.

In contrast with the above claim features, *Wang* provides a vector coprocessor that includes a set of three parallel, paired execution units (each being a combination of a two-input ALU and a two-input MLU and each yielding two outputs, one from each of the ALU and MLU – FIG. 3). Wang's system "targets vectors of length 3, and exploits the intrinsic parallelism by providing **three** parallel **execution units** that can simultaneously operate on all three vector components." Wang emphasizes a three-wide data path for its vector coprocessor, which data path is supported by its **three-wide register file** including register files 40, 42, and 44 (*see*, e.g., Column 8, line 48-53). Thus, Wang discloses and emphasizes a three wide coprocessor that includes a three wide register file to execute vector instructions.

However, a three wide data path from three register files, individually providing **two (2) inputs** to respective ones of **three (3) parallel, paired execution units** is not synonymous with nor teaches *a pair (2)* of execution units that each receive *three (3) operand instructions* or a 3-input unit.

Matsuo also fails to teach or suggest the pair of three input arithmetic units, which receive three operands from two register files. *Matsuo* at col. 27, lines 47 - 52 provides a "3-operand instruction," which is "[a] 'mac' instruction for multiply-add operation." This 3-operand instruction is the instruction **received by** the processing unit for execution and completes the multiplication of two register values (Rsrc1 and Rsrc2) followed by addition of "the value in the pair of registers specified by Rdest" to the result of the multiplication. Notably, the functional description of the execution of the 3-operand instruction makes clear that the 3-operand instruction of *Matsuo* does not simultaneously provide three operands to a single 3-input arithmetic unit or, for that matter, to two such 3-input arithmetic units. Rather, only two operands are provided to the (second) operating unit at a time.

The combination of references fails to suggest the above (and other) features recited by Appellant's example Claim 4. The rejection of Appellant's Claim 4 is thus not well founded and should be reversed. Likewise, Appellant respectfully submits that the rejections of dependent Claim 22, which depends from Claim 4, and Claim 10, which also depend from Claim 1, are not well founded and should be reversed.

Claims 25 and 31 (and 26-30, 32-24)

The rejections of Claims 25 and 31 should also be reversed for the same reasons provided above. Claim 25 recites: "primary and secondary calculating units, wherein the primary **calculating unit includes** first, second, **and third inputs** to receive, respectively, first, second, **and third operands** of a first set of operands and wherein the secondary calculating unit includes first, second, **and third inputs** to receive, respectively, first, second, **and third operands** of a second set of operands; and multiplexing circuitry controlled by the opcode to **select** each of the first, second, **and third operands** ... from the set of primary and secondary file registers..." (*emphasis added*).

Claim 31 recites: "asymmetric instruction includes a set of **three operand register fields** ... wherein the execution unit is configured to perform **a first operation** on a first set of **three operands selected from registers** identified ... and to perform a second operation on a second set of **three operands also selected from the registers**..." (*emphasis added*).

Neither *Wang* nor *Matsuo*, individually or in combination, would suggest to one skilled in the art at the time of Appellant's invention the above features of Appellant's claims. The failures with respect to both *Wang* and *Matsuo* have been explained above (see arguments for Claim 1 and 4). The combination of these references thus fails to suggest several features (as described above) that are recited by Appellant's claims, including the above features recited by Claims 25 and 31, respectively. As such, one skilled in the art would not find Appellant's Claims 25 or 31 unpatentable over the combination of references. The rejections of Claims 25 and 31, as well as Claims 26-30 and Claims 32-34, which respectively depend from these base claims, are therefore not well founded and should be reversed.

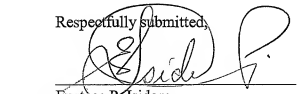
Claim Objections in Final Action

Appellant notes that Examiner retained the objections to Claims 24 and 32 in the present Final Action. However, the informalities were removed by the amendment filed on January 19, 2007. The objections are thus rendered moot.

CONCLUSION

Appellants have pointed out with specificity the manifest error in the Examiner's rejections, and the claim language which renders the invention patentable over the various combinations of references. Appellants, therefore, respectfully request that this case be remanded to the Examiner with instructions to issue a Notice of Allowance for all pending claims.

Respectfully submitted,



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APPENDIX

1. A microprocessor, comprising:

a vector unit to execute a vector instruction to perform a first operation on a first set of operands and a second operation on a second set of operands;

a vector register file comprising a primary register file and a secondary register file;

wherein the vector instruction includes a first register field indicative of a first primary register in the primary register file and a first secondary register in the secondary register file, a second register field indicative of a second primary register in the primary register file and a second secondary register in the secondary register file, and a third register field indicative of a third primary register in the primary register file and a third secondary register in the secondary register file; and

wherein the first set of operands includes a first operand selected from the first primary register or the first secondary register, a second operand selected from the second primary register or the second secondary register, and a third operand selected from the third primary register or the third secondary register.

2-3.

4. The microprocessor of claim 1, wherein the vector unit includes a 3-input primary unit and a 3-input secondary unit, wherein the primary unit is configured to perform the first operation on the first set of operands and the 3-input secondary unit is configured to perform the second operation on the second set of operands.

5-6.

7. The microprocessor of claim 1, wherein the first and second operations use at least one operand from the primary register file and at least one operand from the secondary register file.

8. The microprocessor of claim 1, wherein the first and second sets of operands include at least one common operand.

9. The microprocessor of claim 1, wherein the vector register file contains information representing a real portion of a complex number in the primary register file and an imaginary portion of the complex number in the secondary register file.

10. The microprocessor of claim 9, wherein the vector unit is configured to execute a complex computation instruction in which the imaginary portion of the first operand of the first set of operands is multiplied by an imaginary portion of a second operand in the first operation and in which the imaginary portion of the first operand is multiplied by a real portion of the second operand in the second operation.

11-20. (canceled)

21. The microprocessor of claim 1, wherein the second set of operands include a first operand selected from the first primary register or the first secondary register, a second operand selected from the second primary register or the second secondary register, and a third operand selected from the third primary register or the third secondary register.

22. The microprocessor of claim 4, wherein the first operation includes multiplying two of the three first set of operands to obtain a first product and adding or subtracting the remaining of the first set of operands to or from the first product and wherein the second operation includes multiplying two of the three second set of operands to obtain a second product and adding or subtracting the remaining of the second set of operands to or from the second product.

23. The microprocessor of claim 22, wherein the first and second sets of operands comprise first and second sets of floating point formatted operands.

24. The microprocessor of claim 1, wherein the vector instruction includes a target register field indicative of a primary target register in the primary register file and a secondary target register in the secondary register file and further wherein the vector unit is further configured to store a result of the first operation in the primary target register and to store a result of the second operation in the secondary target register.

25. A vector unit to process a vector instruction having an opcode and first, second, and third register fields, comprising:

a register file including a primary register file having a set of primary registers and a secondary register file having a set of secondary registers, wherein each register field identifies a register in the primary register file and a corresponding register in the secondary register file;

primary and secondary calculating units, wherein the primary calculating unit includes first, second, and third inputs to receive, respectively, first, second, and third operands of a first set of operands and wherein the secondary calculating unit includes first, second, and third inputs to receive, respectively, first, second, and third operands of a second set of operands; and

multiplexing circuitry controlled by the opcode to select each of the first, second, and third operands in the first and second set of operands from the set of primary and secondary file registers identified by the register fields.

26. The vector unit of claim 25, wherein the multiplexing circuitry is controlled by the opcode to select:

the first operand in the first set of operands from either the first primary or the first secondary registers;

the second operand in the first set of operands from either the second primary or the second secondary registers; and

the third operand in the first set of operands from either the third primary or the third secondary registers;

the first operand in the second set of operands from either the first primary or the first secondary registers,

the second operand in the second set of operands from either the second primary. or the second secondary registers; and

the third operand in the second set of operands from either the third primary or the third secondary registers

27. The vector unit of claim 25, wherein the primary calculating unit is controlled by the opcode to perform a first operation on the first set of operands and the secondary calculating unit is controlled by the opcode to perform a second operation on the second set of operands.

28. The vector unit of claim 27, wherein the first operation differs from the second operation.

29. The vector unit of claim 27, wherein the first and second operations both include multiplying their respective first and third operands to obtain respective first products and adding or subtracting their respective second operands to or from the respective first products.

30. The vector unit of claim 25, wherein the first, second, and third operands of the first and second sets of operands are all floating point formatted operands.

31. A microprocessor including:

an execution unit enabled to execute an asymmetric instruction, wherein the asymmetric instruction includes a set of three operand register fields and a target register field and an operation code (opcode);

a register file accessible by the execution unit and having a rank of two including a primary register file and a secondary register file wherein a value in an operand register field identifies a register in the primary register file and a corresponding register in the secondary register file;

wherein the execution unit is configured to perform a first operation on a first set of three operands selected from registers identified by the set of operand register fields and to perform a second operation on a second set of three operands also selected from the registers

identified by the set of operand registers fields wherein the first and second operations and selection of the first and second sets of operands are determined by the opcode.

32. The microprocessor of claim 31, wherein at least one condition selected from a group of conditions consisting of the first and second operations being different and the first and second sets of operands being different is true.

33. The microprocessor of claim 31, wherein the execution unit is further configured to store a result of the first operation in a register of the primary register file determined by the target register field and the result of the second operation in a register of the secondary register field also determined by the target register field.

34. The microprocessor of claim 31, including multiplexing circuitry controlled by the opcode to select a first of the first set of three operands from a first primary and a first secondary register identified by a first operand register field, a second of the first set of three operands from a second primary and a second secondary register identified by a second operand register field, a third of the first set of three operands from a third primary and a third secondary register identified by a first operand register field, a first of the second set of three operands from a first primary and a first secondary register identified by a first operand register field, a second of the second set of three operands from a second primary and a second secondary register identified by a second operand register field, and a third of the second set of three operands from a third primary and a third secondary register identified by a first operand register field.

EVIDENCE APPENDIX

Other than the Office Action(s) and reply(ies) already of record, no additional evidence has been entered by Appellants or the Examiner in the above-identified application which is relevant to this appeal.

RELATED PROCEEDINGS APPENDIX

There are no related proceedings as described by 37 C.F.R. §41.37(c)(1)(x) known to Appellants, Appellants' legal representative, or assignee.